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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,326	01/31/2002	Steven Teig	SPLX.P0110	9826

23349 7590 08/05/2003
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EXAMINER

SIEK, VUTHE

ART UNIT PAPER NUMBER

2825

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,326	TEIG ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on _____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
 5) Claim(s) ____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) ____ is/are objected to.
 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 January 2002 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on ____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. This office action is in response to application 10/066,326 filed on 1/31/2002.

Claims 1-20 remain pending in the application.

Specification

2. The disclosure is objected to because of the following informalities: this application has claimed priority under U.S.C. 119(e) of U.S. Provisional Application No. 60/315,867 and 60/315,834. Therefore, cross-reference to related application should be inserted under the title on a first paragraph of the first page.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dewey et al. (6,430,729).

5. As to claim 1 and 10, Dewey et al. a process and system for maintaining 3 sigma process tolerance for parasitic extraction with on-the-fly biasing. The objective the patent is to provide a structure and method for determining characteristic of parasitic elements (R, C parasitics) in an IC layout comprising identifying manufacturing process

parameters (including a size, spacing, length, width of the wiring) and impacting devices in the IC, calculating a parasitic performance distribution for each of the devices based on the manufacturing process parameters, combining the parasitic performance distribution for each of the devices in a net parasitic value, and performing a parameterized model based on the net parasitic values. The calculating of the parasitic performance distribution includes simultaneously calculating a range of parasitic values for each of the devices based on the manufacturing process parameters. The range of values includes a best case parasitic value, a worst case parasitic value and a nominal parasitic value (the range values are considered to be trained data). The invention allows timing tool not only to consider the three situations for which the geometry of the conductors and wires was created, but also all situations in between; also multiple runs are possible to statically evaluate all possible combinations of parasitic values with "Monte Carlo" techniques (see summary). The process allows deriving parasitic performance values for the devices for the best, worst, and nominal parasitic values from the parameterized model (a parameterized model is considered to be a machine-learning model trained with Bayesian inference implemented with a Monte Carlo method) (see summary, col. 2, line 62 to col. 8, line 58).

6. As to claims 2-9 and 12-20, Dewey et al. teach said electrical characteristic comprises capacitance (capacitance parasitic); resistance (resistance parasitic); extracted sub problem comprising a net, a section of interconnect wiring (Figs. 2-3); one of set of physical parameters comprising a distance between a pair of interconnect lines (spacing d), a wire width, a wire length (cols. 3-4); selecting said machine-learning

model from a plurality of machine-learning models (parameterized models for parasitic elements, see summary; the range of values including a best case parasitic value, a worst case parasitic value and a nominal parasitic value; using these values to derive parasitic performance values for the devices from the parameterized model); determining a capacitance per unit length and multiplying said capacitance per unit length by a length of the subsection of the interconnect wiring (capacitance in function length, width, space, pattern density) (col. 4; see summary).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek
Primary Examiner
July 17, 2003

Vuthe Siek
VUTHE SIEK
PRIMARY EXAMINER